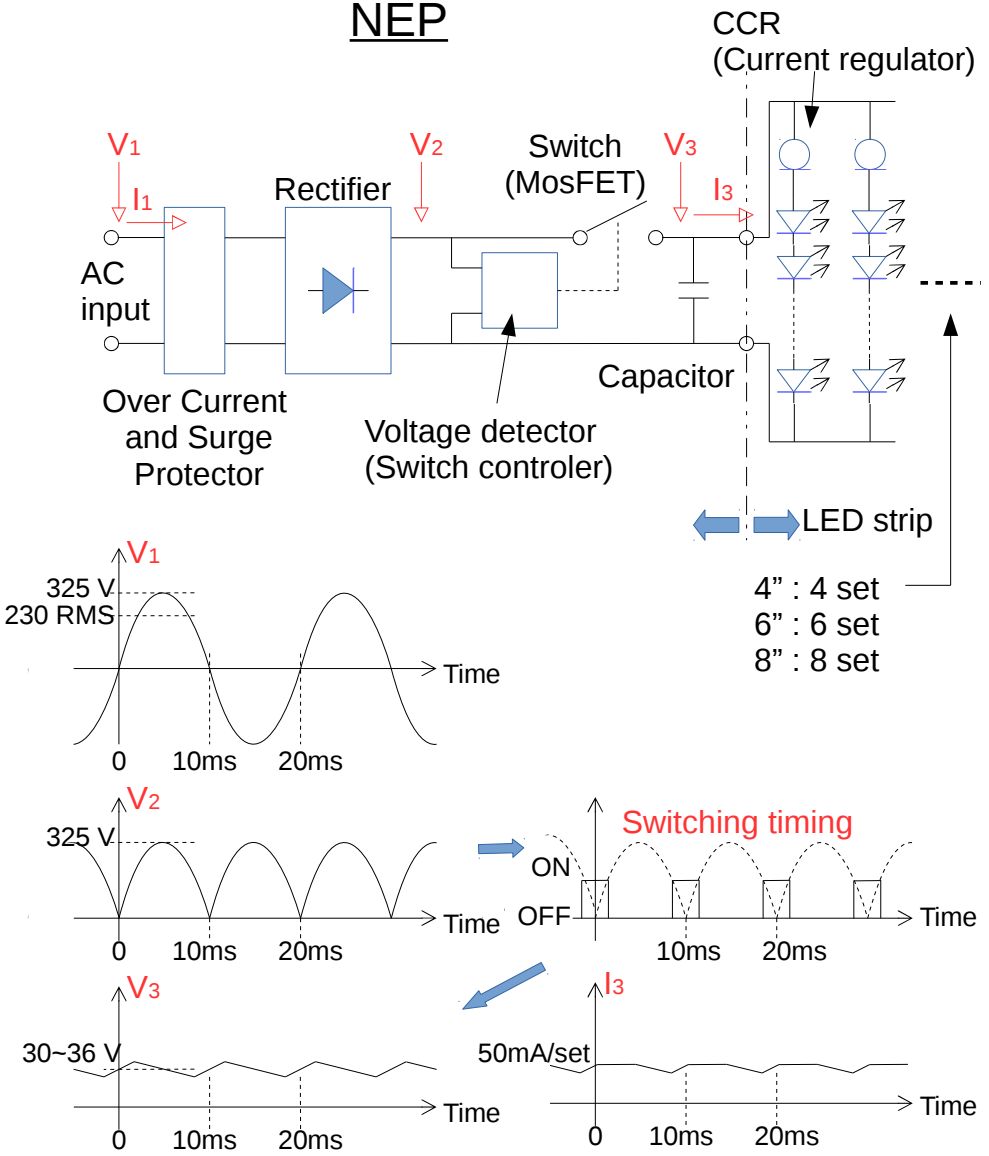
NEP (NSP-EASTOOL Power supply circuit)

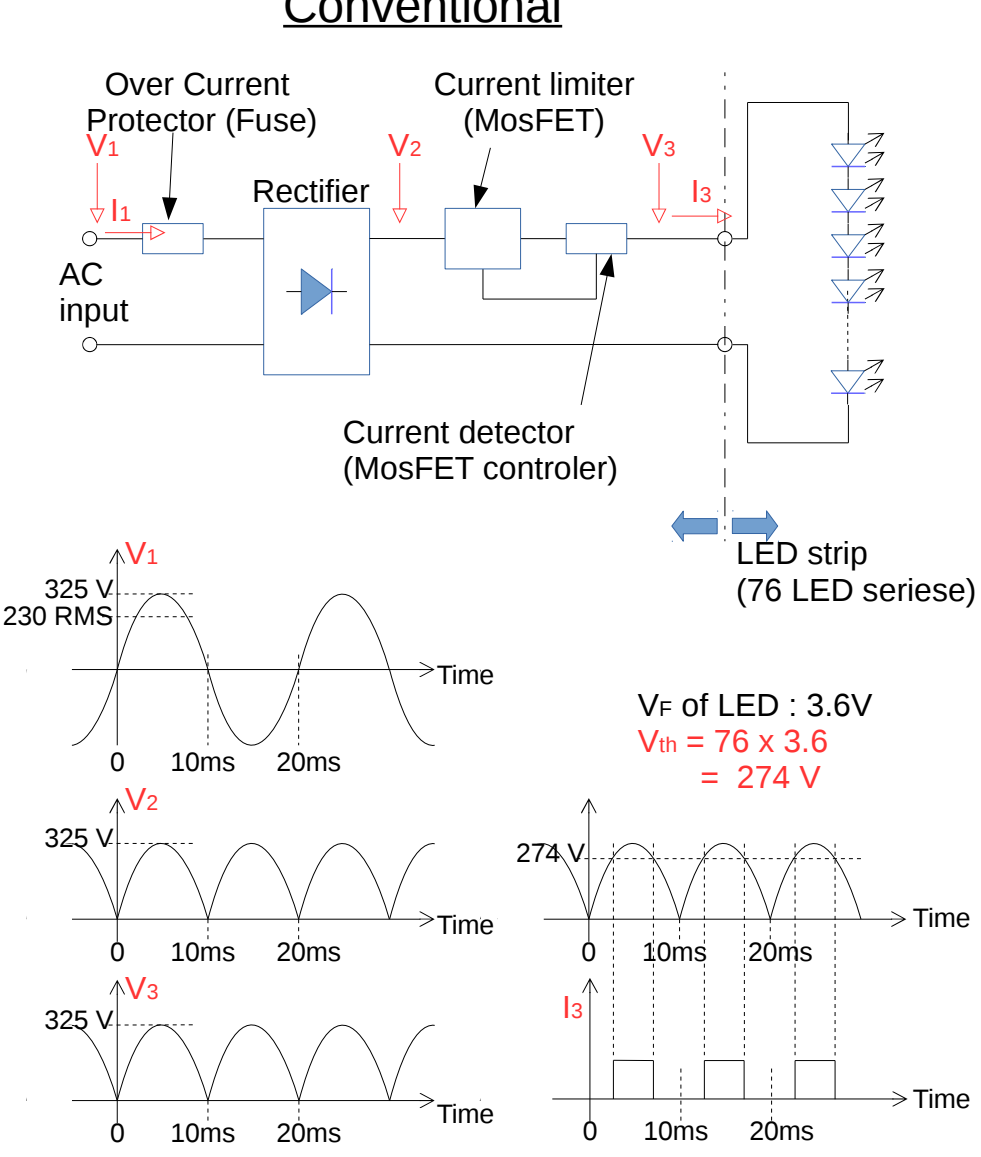
16/Aug/2014 by K.Yamauchi

Operating diagram

NEP

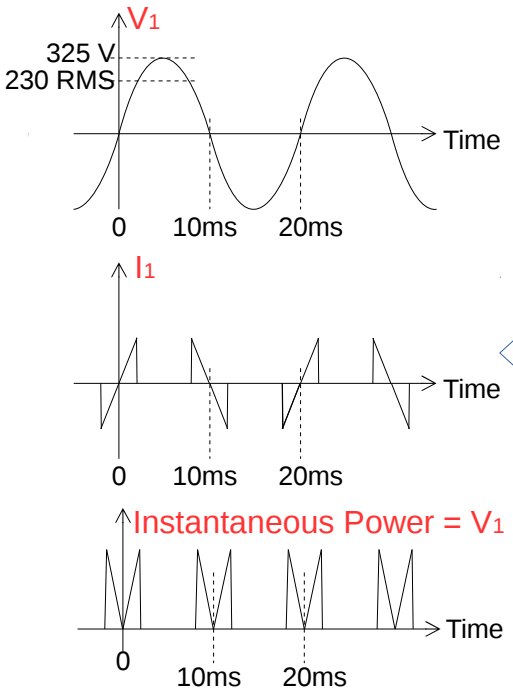


Conventional



Power Factor and Power line current harmonics

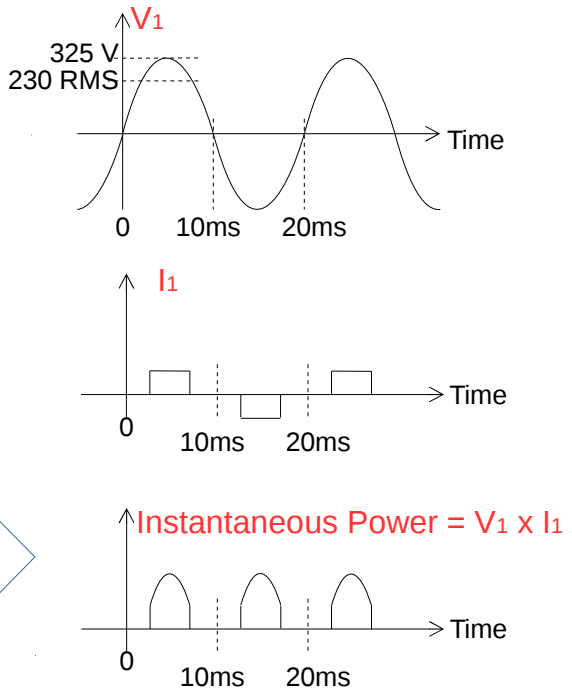
NEP



Higher harmonics

Area to be same
for same Power

Conventional



Higher harmonics means Lower Power Factor.

What is the advantage of NEP?

Power Factor pattern of electric components.
A (100% PF) : Incandescent lamp, Steam Iron, Traditional heater, Traditional cooking stove, etc.
B (10 ~ 90% PF) : TV, PC, Fluorscent lamp, etc. (Almost all equipments are here)
C (Higher PF but higher harmonics level) : Inverter AC, etc.
D (Low PF but no harmonics) : Motors – only phase shifted current waveform

Why type B indicates lower PF?
Almost all electric equipments are working with DC.
Conventional AC/DC converter make PF lower because it is so called “Capacitor Input”.
Only when input voltage is higher than capacitor voltage, current goes into circuit.
In other words, these equipments are discarding low voltage area of AC input.

To improve PF (or to reduce harmonics), recent AC/DC converter includes PFC (Power Factor Correction) circuit.
This PFC circuit is designed to consume the low voltage area of AC input with trading off of efficiency.

This idea is exactly same concept as our “NEP” LED driver circuit.
Difference is that PFC is targeting own equipment but “NEP” is targeting all electrical equipments total PF in a residence.

Note : Because we can not fix the target equipments in a residence, this PF improvement is not guaranteed always.